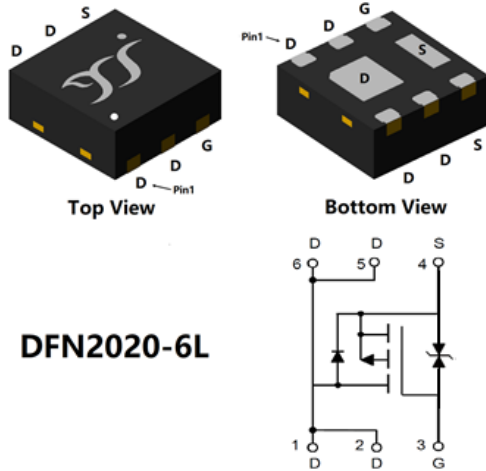


P-Channel Enhancement Mode Field Effect Transistor



DFN2020-6L

Product Summary

- V_{DS} -60V
- I_D -5.6A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <169m Ω
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <246m Ω
- ESD Protected Up to 2KV (HBM)

General Description

- Voltage controlled small signal switch
- Low input capacitance
- Fast switching speed
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Reverse polarity protection
- Load switch

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	-60	V
Gate-source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} =-10V	I _D	-	-2.1	A
		T _A =100°C,V _{GS} =-10V		-	-1.3	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C,V _{GS} =-10V,Chip limitation		-	-5.6	
		T _C =100°C,V _{GS} =-10V		-	-3.5	
Pulsed Drain Current	T _C =25°C,t _p ≤10μs		I _{DM}	-	-22.4	
Maximum Body-Diode Continuous Current	T _C =25°C		I _S		-5.6	
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	1.5	W
		T _A =100°C		-	0.6	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	10.4	
		T _C =100°C		-	4.2	
Junction and Storage Temperature Range			T _J ,T _{STG}	-55	150	°C

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	82	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	12	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQT169P06AK	F1	169P06	3000	30000	120000	7" reel



YJQT169P06AK

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA, T _j =25°C	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V, T _j =25°C	-	-	-1	μA
		V _{DS} =-60V, V _{GS} =0V, T _j =150°C	-	-	-100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V, T _j =25°C	-	-	±10	μA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA, T _j =25°C	-1.1	-1.6	-2.1	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-1.5A, T _j =25°C	-	126	169	mΩ
		V _{GS} =-4.5V, I _D =-0.7A, T _j =25°C	-	164	246	mΩ
Diode Forward Voltage	V _{SD}	I _S =-1.2A, V _{GS} =0V, T _j =25°C	-	-0.81	-1.2	V
Gate Resistance	R _G	f=1MHz, T _j =25°C	-	7.7	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, f=1MHz, T _j =25°C	-	414	-	pF
Output Capacitance	C _{oss}		-	31.4	-	
Reverse Transfer Capacitance	C _{rss}		-	24.4	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-30V, I _D =-1.5A, T _j =25°C	-	10.6	-	nC
Gate-Source Charge	Q _{gs}		-	1	-	
Gate-Drain Charge	Q _{gd}		-	1.9	-	
Reverse Recovery Charge	Q _{rr}	I _F =-1.5A, di/dt=100A/μs, V _{GS} =0V, V _R =-30V, T _j =25°C	-	19.3	-	nC
Reverse Recovery Time	t _{rr}		-	19.1	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DS} =-30V, I _D =-1.5A, R _{GEN} =3Ω, T _j =25°C	-	5.9	-	ns
Turn-on Rise Time	t _r		-	2.9	-	
Turn-off Delay Time	t _{D(off)}		-	20.4	-	
Turn-off Fall Time	t _f		-	4.6	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



■ Typical Electrical and Thermal Characteristics Diagrams

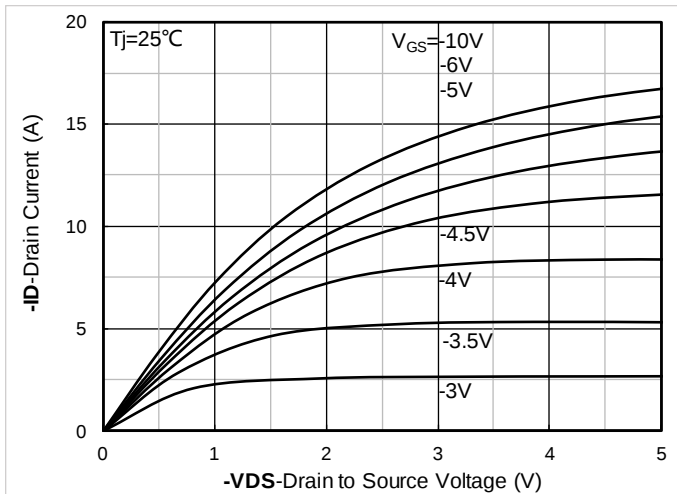


Figure 1. Output Characteristics; typical values

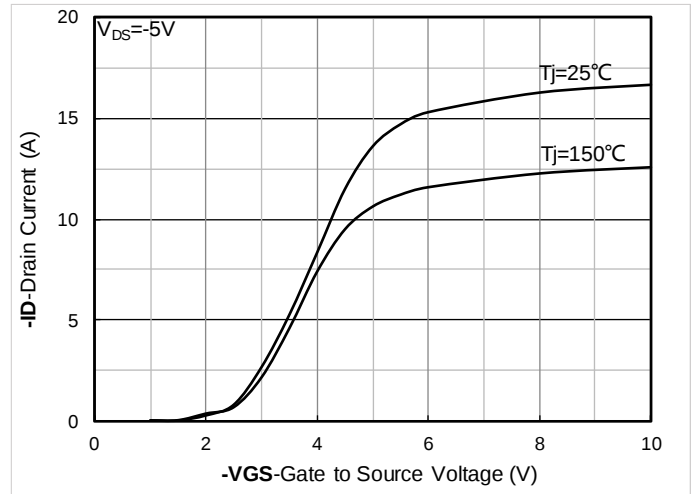


Figure 2. Transfer Characteristics; typical values

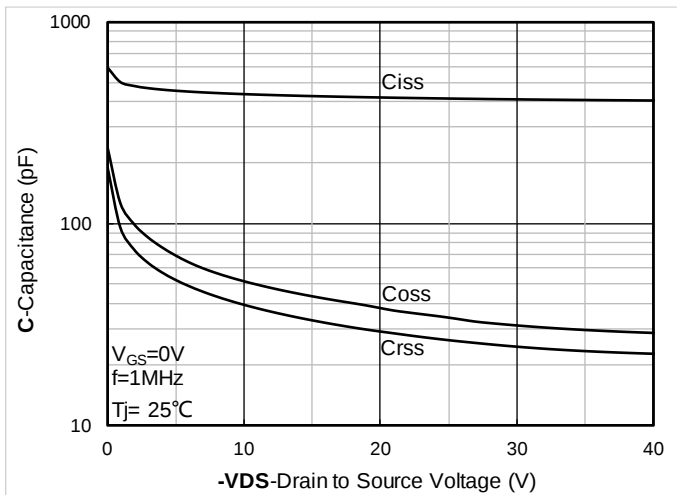


Figure 3. Capacitance Characteristics; typical values

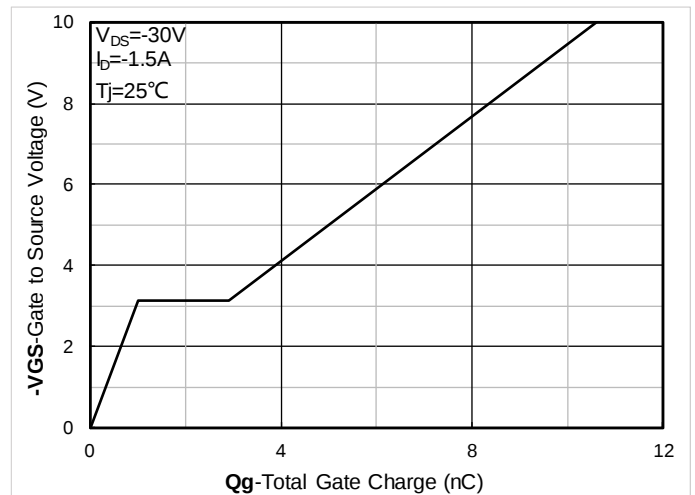


Figure 4. Gate Charge; typical values

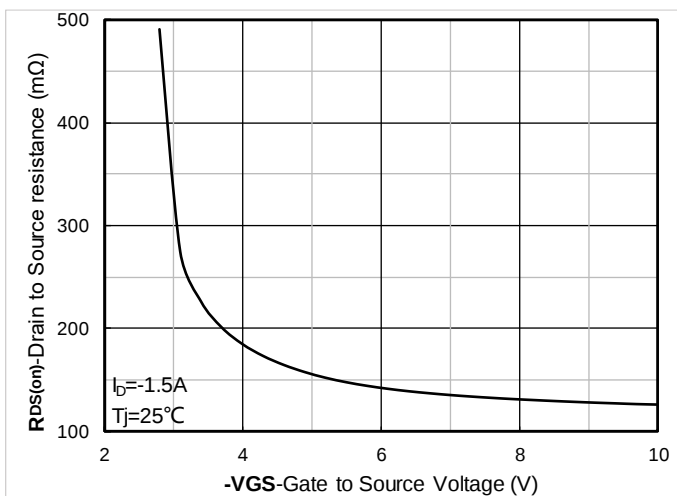


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

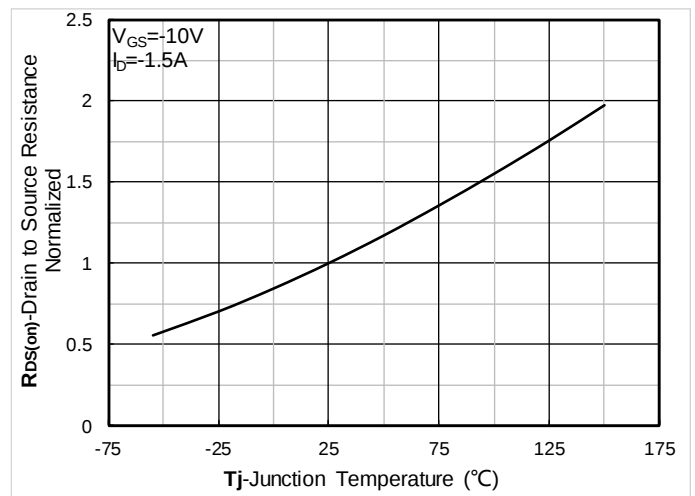


Figure 6. Normalized On-Resistance

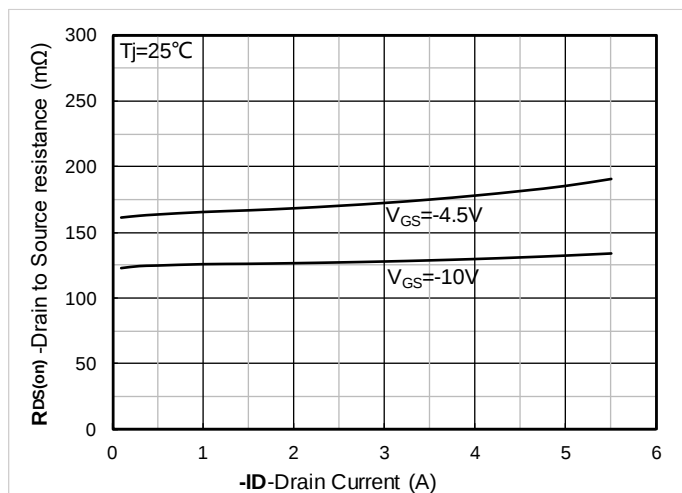


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

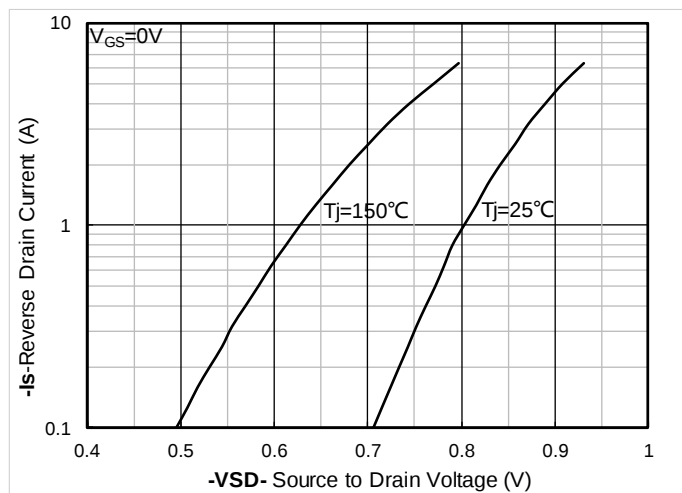


Figure 8. Forward characteristics of reverse diode; typical values

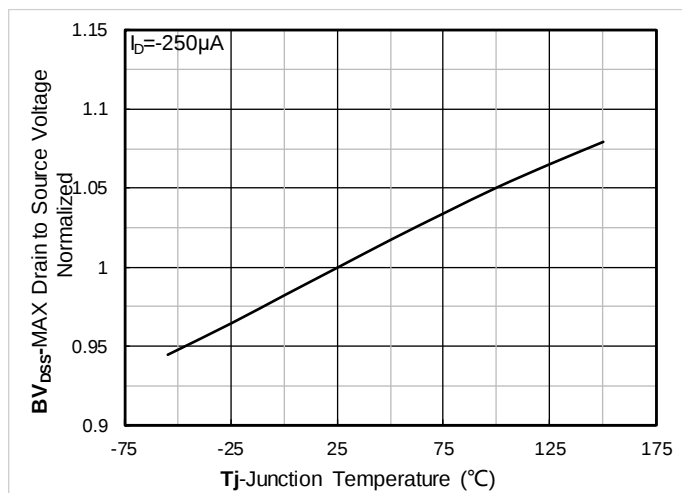


Figure 9. Normalized breakdown voltage

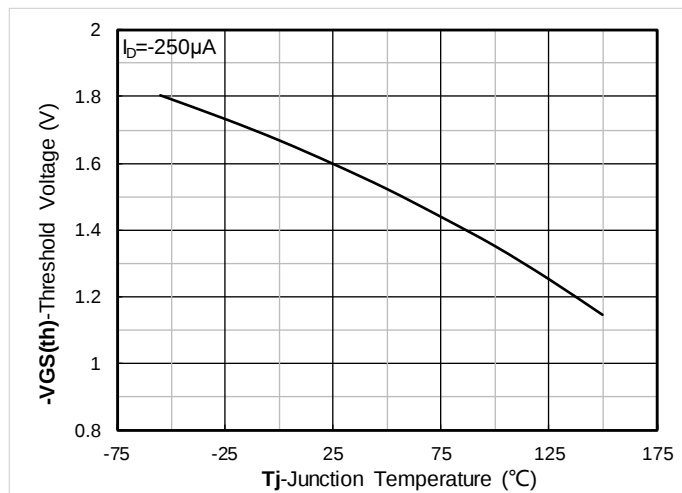


Figure 10. Gate Threshold voltage; typical values

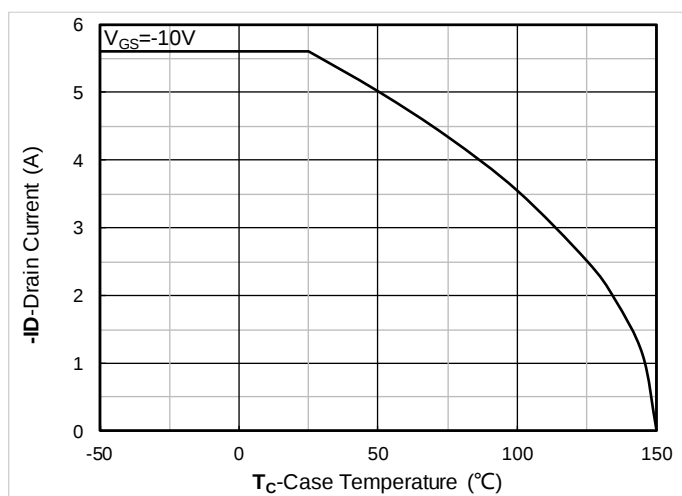


Figure 11. Current dissipation

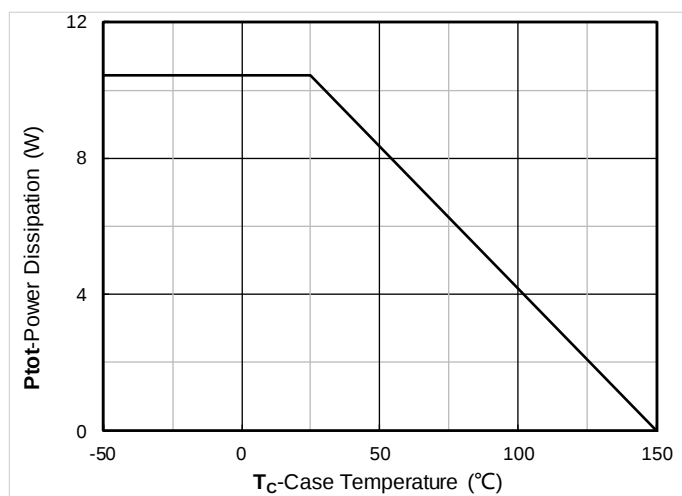


Figure 12. Power dissipation

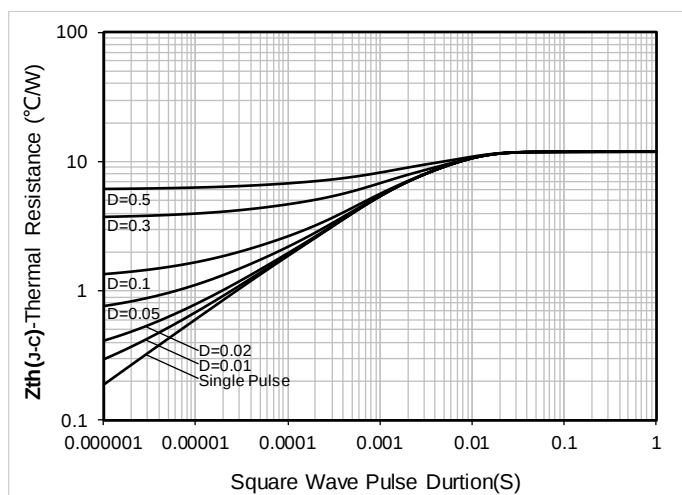


Figure 13. Maximum Transient Thermal Impedance

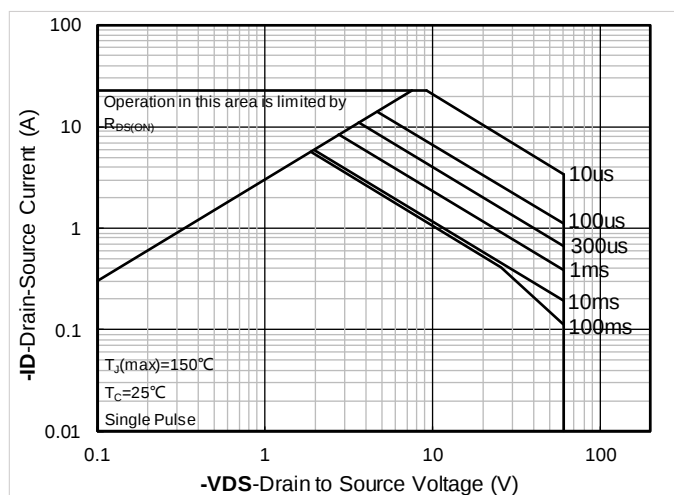
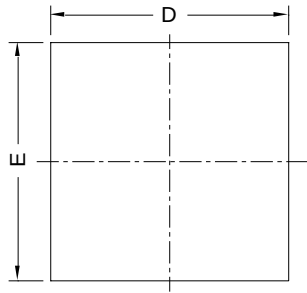


Figure 14. Safe Operation Area

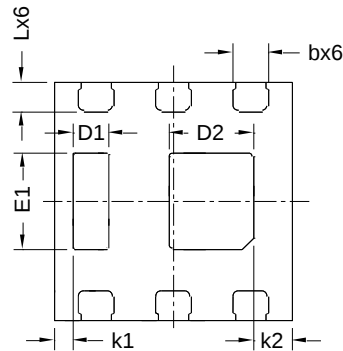


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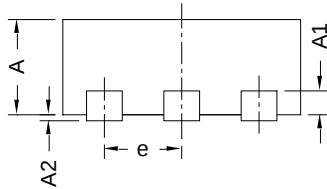
■ DFN2020-6L-E-0.8MM Package information



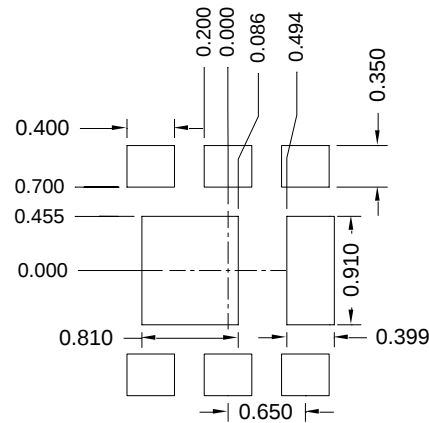
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e	0.65 BSC		
k1	0.156 BSC		
k2	0.326 BSC		

Note:

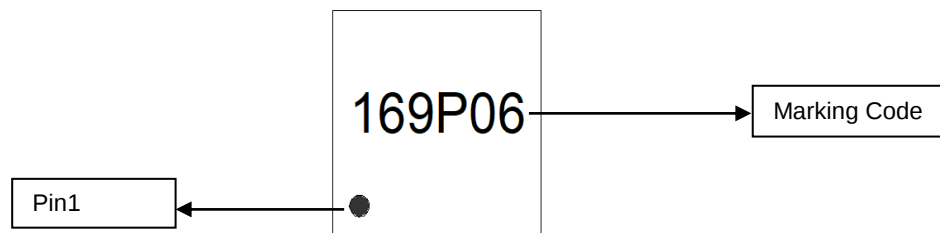
1.Controlling dimension:in millimeters.

2.General tolerance:±0.10mm.

3.The pad layout is for reference purposes only.



■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. 169P06 is marking code
4. Body color: Black



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